Claims

1. A code division multiple access (CDMA) system comprising:

at least one CDMA transmitter having:

at least one spreader for spreading a packet having one or more blocks to derive an M x G spread sequence for each of said blocks to thereby form a spread signal, where M represents number of symbols, said number being greater or equal to one, each of said at least one spreader having a processing gain of G;

and

a sequence extender for extending each of said blocks using a predetermined number of chips to thereby form an extended spread signal, said sequence extender having an extender input coupled to said spreader output.

2. The CDMA system of Claim 1, wherein said packet comprises a plurality of pilot chips.

3. The CDMA system of Claim 2, wherein said plurality of pilot chips is placed together as one or more pilot blocks within said packet.

4. The CDMA system of Claim 2, wherein said plurality of pilot chips is dedicated to a single user.

5. The CDMA system of Claim 2, wherein said plurality of pilot chips is common to one or more users in a transmission of said extended spread signal.

6. The CDMA system of Claim 2, wherein pilot chips within each of said blocks are equally spaced in a transmission of said extended spread signal.

7. The CDMA system of Claim 6, wherein said pilot chips within each of said blocks are determined based upon data from said each of said blocks.

8. The CDMA system of Claim 7, wherein said pilot chips is determined based upon $p= A^{-1}(\alpha g - Bd)$, where p is a pilot vector in the time domain, g is a known spreading sequence for channel estimation, d is the sum of spread data of all users, α is a scalar value based upon data in said blocks, and A and B are sub-matrices derived from Fast Fourier Transform based upon positions of p and g.

9. The CDMA system of Claim 2, wherein said sequence extender is adapted to extract said predetermined number of chips from a tail portion of each of said blocks for placing in front of said each of said blocks.

10. The CDMA system of Claim 2, wherein said sequence extender is adapted to extract said predetermined number of chips from a head portion and a tail portion of each of said blocks, said predetermined number of chips from said head portion being placed behind said tail portion and said predetermined number of chips from said tail portion being placed behind said tail portion.

11. The CDMA system of Claim 2, wherein said sequence extender is adapted to insert said predetermined number of chips as zeros after each of said blocks.

12. The CDMA system of Claim 2, wherein said sequence extender is adapted to insert said predetermined number of chips as zeros before and after each of said blocks.

13. The CDMA system of Claim 1, wherein said CDMA transmitter further comprises a combiner having a combiner input and a combiner output, said combiner input being coupled to said spreader output of each of said at least one spreader, said combiner output being coupled to said extender input.

14. The CDMA system of Claim 1, wherein said transmitter further comprises a pulse shaper, coupled to output of said sequence extender.

15. A method for transmitting signals in a code division multiple access (CDMA) system, said method comprising the steps of:

spreading, by at least one spreader, a packet having one or more blocks to derive an M x G spread sequence for each of said blocks to thereby form a spread signal, where M represents number of symbols, said number being greater or equal to one, each of said at least one spreader having a processing gain of G;

and

extending, by a sequence extender, said M x G spread sequence using a predetermined number of chips to thereby form an extended spread signal, said M x G spread sequence being received from a spreader output of each of said at least one spreader.

16. The method of Claim 15, and further comprising the step of multiplexing a plurality of pilot chips with data of said packet before said spreading step.

17. The method of Claim 16, wherein said multiplexing step comprises the step of placing said plurality of pilot chips together as one or more pilot blocks within said packet.

18. The method of Claim 16, wherein said multiplexing step comprises the step of dedicating said plurality of pilot chips to a single user.

19. The method of Claim 16, wherein said multiplexing step comprises the step of setting said plurality of pilot chips to be common to one or more users in a transmission of said extended spread signal.

20. The method of Claim 15, and further comprising the step of determining pilot chips for each of said blocks after said spreading step and before said extending step, said pilot chips being based upon data from said each of said blocks.

21. The method of Claim 20, wherein said determining step comprises the step of multiplexing said pilot chips to be equally spaced within said each of said blocks.

22. The method of Claim 20, wherein said determining step comprises the step of determining said pilot chips based upon $p = A^{-1}(\alpha g - Bd)$, where p is a pilot vector in the time domain, g is a known spreading sequence for channel estimation, d is the sum of spread data of all users, α is a scalar value based upon data in said blocks, and A and B are sub-matrices derived from Fast Fourier Transform based upon positions of p and g.

23. The method of Claim 15, wherein said extending step comprises the step of extracting said predetermined number of chips from a tail portion of each of said blocks for placing in front of said each of said blocks.

24. The method of Claim 15, wherein said extending step comprises the step of extracting said predetermined number of chips from a head portion and a tail portion of each of said blocks, said predetermined number of chips from said head portion being placed behind said tail portion and said predetermined number of chips from said tail portion being placed behind said tail portion.

25. The method of Claim 15, wherein said extending step comprises the step of inserting said predetermined number of chips as zeros after each of said blocks.

26. The method of Claim 15, wherein said extending step comprises the step of inserting said predetermined number of chips as zeros before and after each of said blocks.

27. The method of Claim 15, wherein said spreading step comprises the step of combining output from said at least one spreader.

28. The method of Claim 15, and further comprising the step of pulse shaping said M x G spread sequence after said extending step.

29. A code division multiple access (CDMA) system comprising:

at least one CDMA receiver for processing a received signal, said CDMA receiver having:

a sequence extension remover for removing a predetermined number of chips from at least one predetermined position of said received signal to thereby form a modified signal;

an orthogonal transform block, coupled to said sequence extension remover, for transforming said modified signal in a first domain to form a transformed signal in a second domain;

an equalizer block, coupled to said transform block and having a channel estimator, for equalizing said transformed signal to thereby reduce channel distortion and form an equalized signal;

an inverse orthogonal transform block, coupled to said equalizer block, for inverse transforming said equalized signal to form an output in said first domain;

and

a despreader for despreading said output to thereby derive a group of symbols.

30. The CDMA system of Claim 29, wherein said at least one predetermined position comprises a front portion of each of one or more blocks of said received signal.

31. The CDMA system of Claim 29, wherein said at least one predetermined position comprises a tail portion of each of one or more blocks of said received signal, wherein said sequence extension remover adds said tail portion to a starting portion of said each of one or more blocks, said starting portion having the same number of chips as said tail portion.

32. The CDMA system of Claim 29, wherein said at least one predetermined position comprises a head portion and a tail portion of each of one or more blocks of said received signal.

33. The CDMA system of Claim 29, wherein said at least one predetermined position comprises a front portion and a tail portion of each of one or more blocks of said received signal, wherein said sequence extension remover adds said tail portion to a portion of said each of one or more blocks, said portion having the same number of chips as said tail portion and starts immediately after said front portion in said each of one or more blocks.

34. The CDMA system of Claim 29, wherein said orthogonal transform block comprises a Fast Fourier Transform block, further wherein said first domain is the time domain and said second domain is the frequency domain.

35. The CDMA system of Claim 34, wherein said inverse orthogonal transform block comprises an inverse Fast Fourier Transform block.

36. The CDMA system of Claim 29, wherein said spread signal comprises a plurality of pilot chips.

37. The CDMA system of Claim 36, wherein said spread signal is a transmission to one or more users, said plurality of pilot chips being common to said one or more users.

38. The CDMA system of Claim 36, wherein said spread signal is a transmission to one or more users, said plurality of pilot chips being equally spaced within each of one or more blocks of said spread signal.

39. A method for processing a received signal received in a code division multiple access (CDMA) system, said method comprising the steps of:

removing a predetermined number of chips from at least one predetermined position of said received signal to thereby form a modified signal;

orthogonally transforming said modified signal in a first domain to form a transformed signal in a second domain;

equalizing said transformed signal to thereby reduce channel distortion and form an equalized signal;

inverse orthogonally transforming said equalized signal to form an output in said first domain;

and

despreading said output to thereby derive a group of symbols.

40. The method of Claim 39, wherein said removing step comprises the step of removing said predetermined number of chips from a front portion of each of one or more blocks of said received signal.

41. The method of Claim 39, wherein said removing step comprises the steps of:

removing said predetermined number of chips from a tail portion of each of one or more blocks of said received signal;

and

adding said tail portion to a starting portion of said each of one or more blocks, said starting portion having the same number of chips as said tail portion.

42. The method of Claim 39, wherein said removing step comprises the step of removing said predetermined number of chips from a head portion and a tail portion of each of one or more blocks of said received signal.

43. The method of Claim 39, wherein said removing step comprises the steps of:

removing said predetermined number of chips from a front portion and a tail portion of each of one or more blocks of said received signal;

and

adding said tail portion to a portion of said each of one or more blocks, said portion having the same number of chips as said tail portion.

44. The method of Claim 39, wherein said orthogonally transforming step comprises the step of orthogonally transforming from the time domain as said first domain to the frequency domain as said second domain being.

45. The method of Claim 44, wherein said inverse orthogonally transforming step comprises the step of inverse orthogonally transforming from the frequency domain to the time domain.